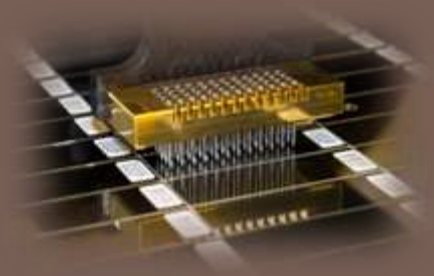
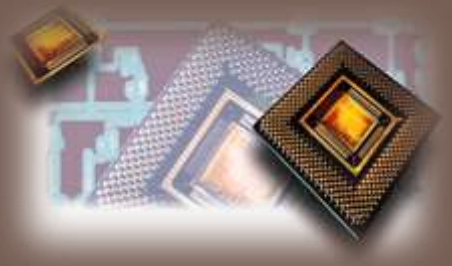
National Institute for Research and Development of Isotopic and Molecular Technologies

FPGA Based Hardware Architectures for High Performance Computing Applications

Authors

Bogdan BELEAN | Sergiu POGACIAN | Adrian BOT





FPGA Based Hardware Architectures for High Performance Computing Applications

- Content

A FPGA Technology Description

B cDNA Microarray image processing

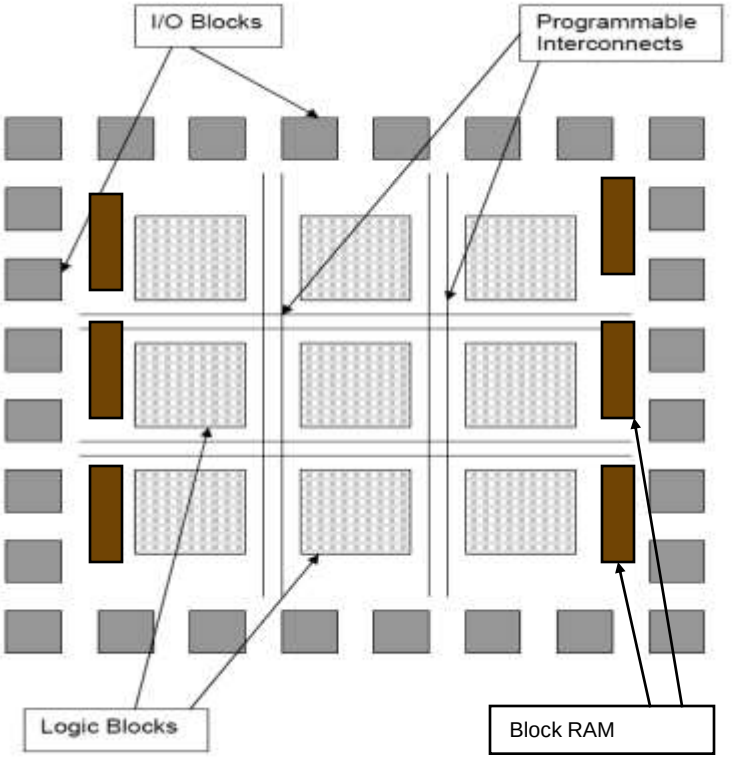
C Low-density Parity Check Codes (Error Correction Codes)

FPGA Technology Description

FPGA

Field Programmable Gate Arrays = digital logic chips containing:

- Configurable Logic Blocks (CLB)
  - LUT (Look Up Table)
  - Multiplexors
  - Flip-Flops
- Programmable interconnects & switch matrices
- I/O Bocks (programmable)
- Block RAMs
- Processors (Power PC)
- Clock



FPGA Technology Description

Major advantage

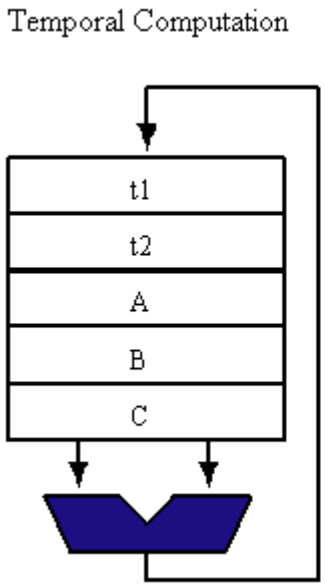
- **Spatial vs. temporal computation**

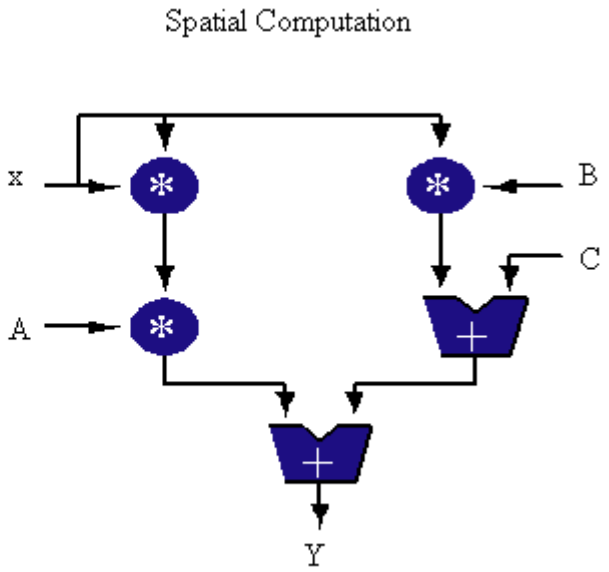
- temporal (serial) **computing** – only one computation can proceed at a time. CPU has to wait while program code or data is fetched.

- spatial is parallel **computing** – one set of gates is processing on part of the algorithm while other gates are doing other tasks.

$Y = Ax^2+Bx+C$

$t_1 = x$
$t_2 = t_1 * A$
$t_2 = t_1 + B$
$t_2 = t_2 * t_1$
$y = t_2 + C$

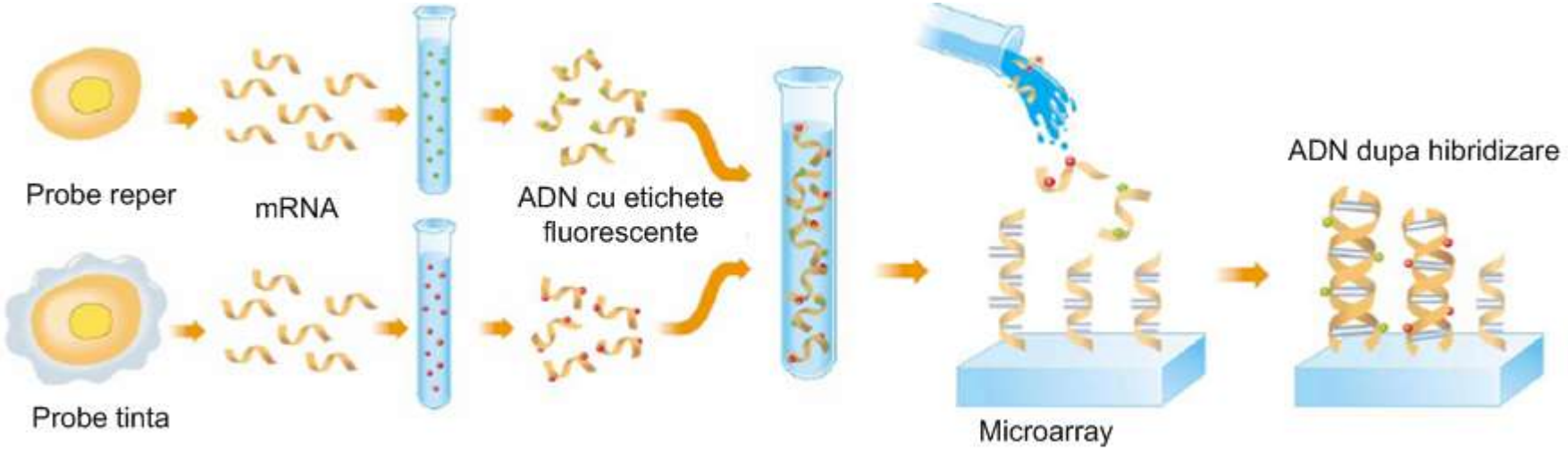




cDNA Microarray image processing

Microarray experiment:

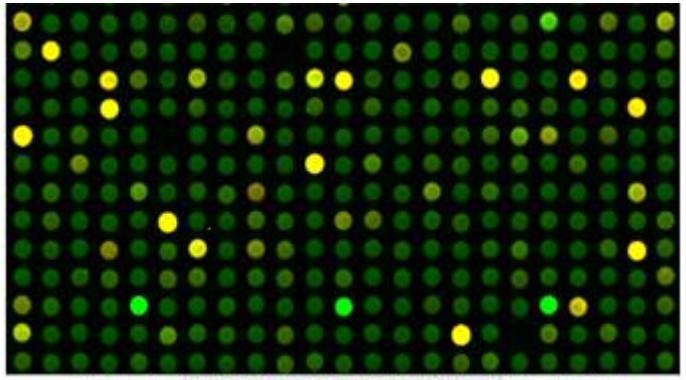
- Prelevarea probelor de cDNA
- Probes labeling (fluorescent markers Cy3, Cy5)
- Hybridization of cDNA probes on microarray glass slide
- Microarray scanning
- Data analysis



cDNA Microarray image processing

- Processing Platforms: *Agilent Feature Extraction Software*, *Agilent GeneSpring*
- GEO database (Gene Expression Omnibus) – images and results

  - Preprocessing
    - Noise removal
    - Image Enhancement
  - Addressing
  - Segmentation
  - Intensity extraction



RAW DATA PARAMETERS FOR "*MUS MUSCULUS*" EXPERIMENT DELIVERED BY AGILENT FEATURE EXTRACTION SOFTWARE

GeneName	PositionX	PositionY	Cy3-Signal	Cy5-Signal
AW919304	507.464	100.106	3.30E+03	4.39E+01
CB547437	528.834	101.483	3.65E+02	4.59E+01
TC554731	550.349	99.906	3.08E+02	6.25E+01
Pro25G	571.669	100.822	3.20E+03	1.51E+03
Tmprss2	592.255	99.8414	3.62E+02	6.45E+01
RGD1304622	613.64	100.673	4.99E+02	8.72E+01
...	...	...	...	...

cDNA Microarray image processing

Microarray printing

- probe cDNA
- printing robot

Microarray Scanning

- double laser scan
- Microarray images

- The necessity of a workstation, a software platform and a bioinformatics engineer have the following disadvantages:
  - High cost
  - Low efficiency regarding the computational time.
- **Soluton:** Developing application specific hardware architectures for automatic microarray image processing.

How does gene expression influence the living organisms evolution and functions

Image processing

-Software platforms

-Bioinformatician

Results analysis

- Gene expression analysis
- diagnose

cDNA Microarray image processing

Image processing methods for automatic microarray image processing

- Preprocessing
  - Enhancing weakly expressed spots

$$I_L(x,y) = \frac{\ln(I_0(x,y)+1)}{\ln 2^n}\cdot 2^n$$

$$I_A(x,y) = \begin{cases} \dfrac{2^n\, atgh(\frac{I(x,y)-k}{k+1})}{atgh(\frac{-k}{k+1})}, I(x,y) <= k; \\ \dfrac{2^n\, atgh(\frac{I(x,y)-k}{2^n})}{atgh(\frac{2^n-1}{2^n})}, I(x,y) > k; \end{cases}$$

- Adressing
  - Shock filters

IN : Image profiles

$$VP(x) = \frac{1}{Y}\sum_{y=0}^{Y-1} I(x,y)$$

$$HP(y) = \frac{1}{X}\sum_{x=0}^{X-1} I(x,y)$$

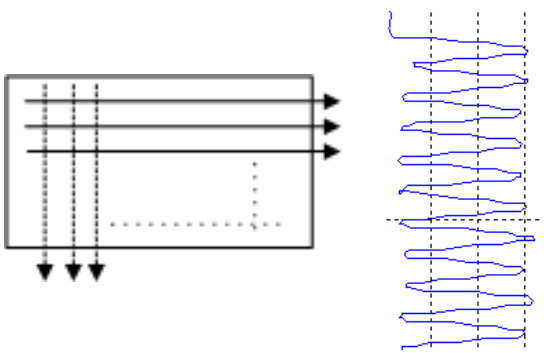
Continuous model

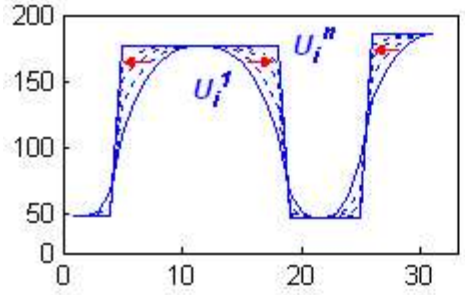
$$U_t = -sign(U_{xx})|U_x|$$

Discrete model

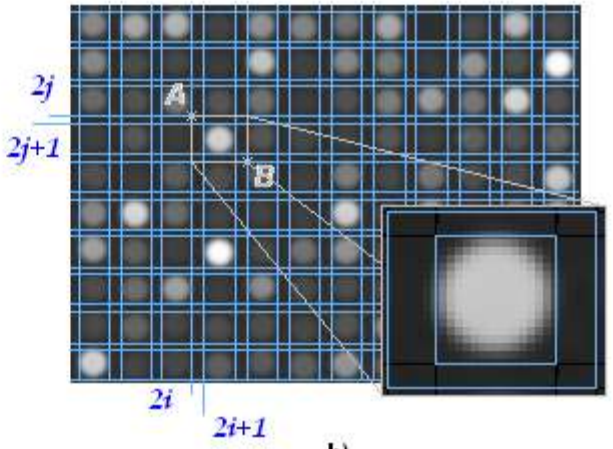
$$U_t = -sign(U_{xx})|U_x|$$

$$U_i^{n+1} = U_i^n - |DU_i^n|\cdot sign(D^2 U_i^n)$$





a)

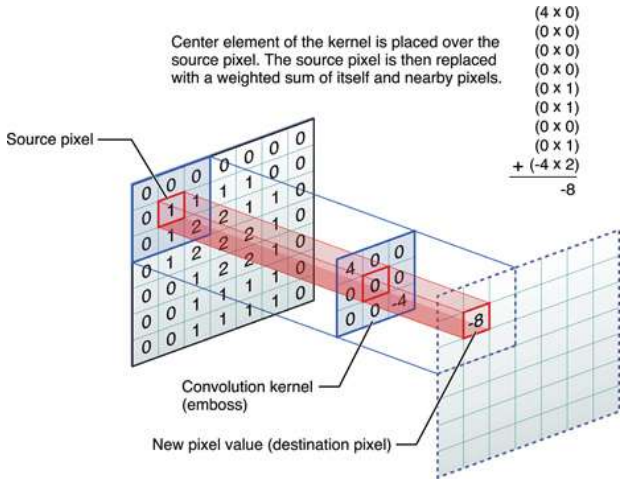


b)

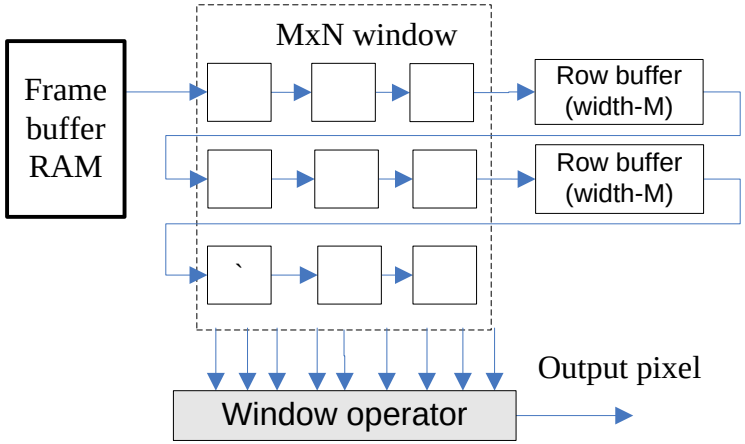
cDNA Microarray image processing

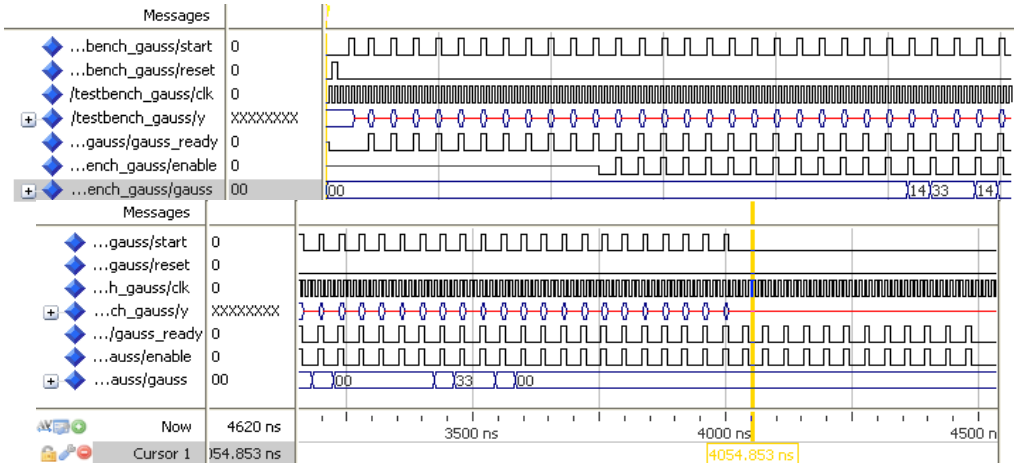
Image processing methods for automatic microarray image processing

- Segmentation
  - Image convolution



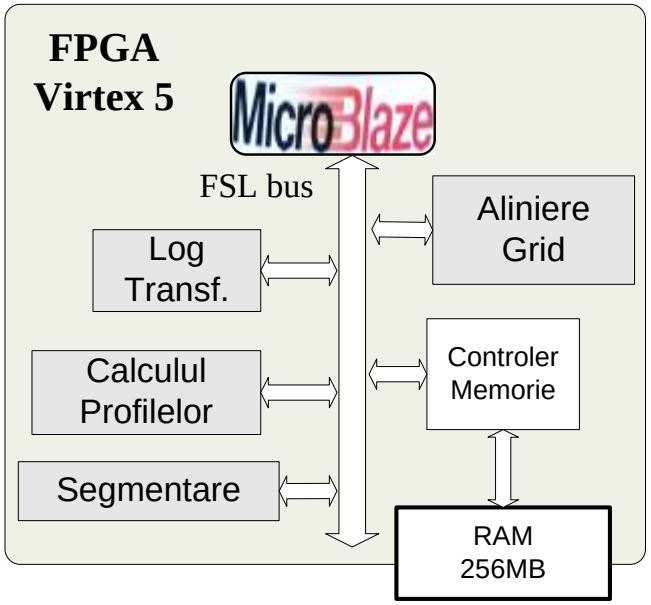
$$\frac{1}{256}\begin{bmatrix} 21 & 31 & 21 \\ 31 & 48 & 31 \\ 21 & 31 & 21 \end{bmatrix} \qquad \frac{1}{115}\begin{bmatrix} 2 & 4 & 5 & 4 & 2 \\ 4 & 9 & 12 & 9 & 4 \\ 5 & 12 & 15 & 12 & 5 \\ 4 & 9 & 12 & 9 & 4 \\ 2 & 4 & 5 & 4 & 2 \end{bmatrix}$$

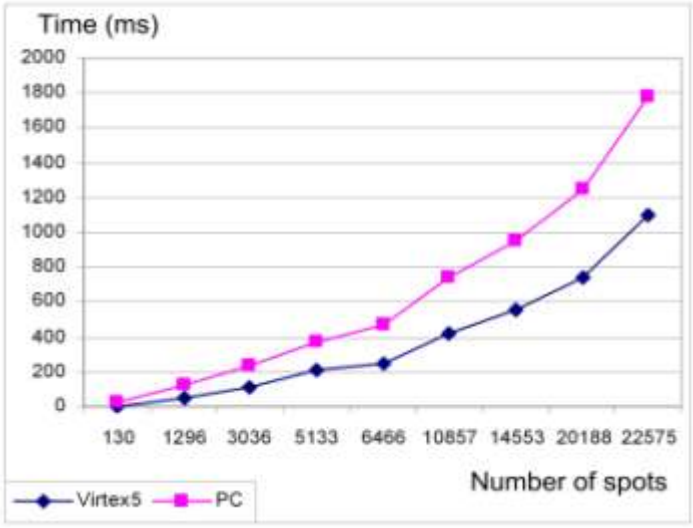




cDNA Microarray image processing

Overall results





Resurse hardware utilizate					
	Transformare Logaritmica	Calcul de profile și adresare (filtre de soc)	Segmentare	**Total**	**Disponibil**
Nr. slice reg.	18	355	1068	**1441**	69120
Nr. slice LUT	-	8525	1736	**10261**	69120
Nr. Block RAM	-	4	2	**6**	148
Nr. BUFG	1	-	1	**2**	32
Nr. DSP48E	4	2	-	**6**	64

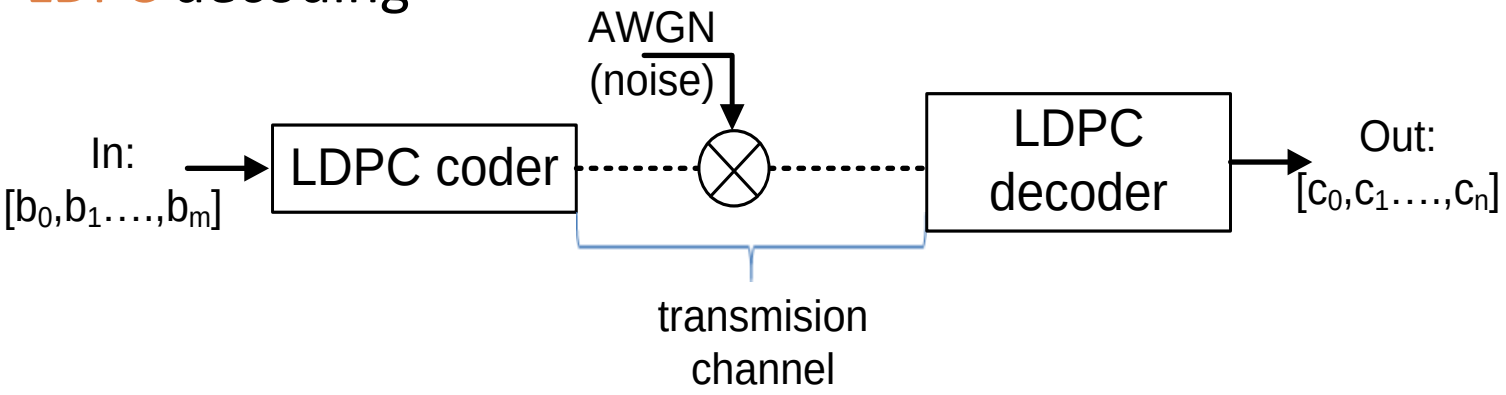
Low density parity check codes

Introduction

- LDPC
  - Introduced by Galager in 1962
  - LDPC codes offer remarkable performances falling only 0.04 dB short of the Shannon theoretical limit
  - insufficient computational power available for the decoding process
  - FPGA/ASIC technologies and digital signal processors, LDPC codes are considered a significant breakthrough in the world of digital communications
  - Standards:
    - WiMAX for wireless networks
    - DVB-S2 for satellite broadcasting services use LDPC codes

Low density parity check codes

- LDPC decoding



  - iterative decoding
  - error correction capacity
  - computationally expensive

Low density parity check codes

LDPC codes

- linear block codes (m,n) where *m = information* bits and *n = total no. of bits* in a codeword
- k = control bits added after encoding

  n = m + k
- encoding relation: $[i] \cdot G_{mxn} = [c]$

  G_{mxn} → Generator matrix
- decoding – based on parity matrix $H_{M,N}$ – sparse matrix
  - Hard decoding
  - Soft decoding – Message passing algorithm (probability propagation)

$H_{M,N}$

- M → no. bits codeword
- N → bits involved in parity check

Low density parity check codes

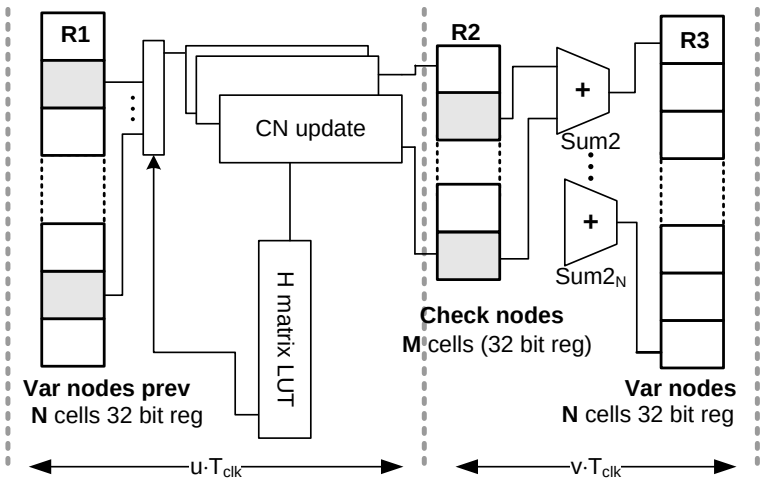
Introduction

- Standards:
  - WiMAX - 576 x 288
  - DVB-S2 - 1022 x 8176

Implementation approach	*Code length (standard)*	*Throughput*
1. GPU	*10 000 bits*	*100Mbps*
1. FPGA/ASIC	*2048b*	*240 Mbps*
	672b (~WiMAX)	*822 Mbps*
	64800b (DVB-S2)	*520 Mbps*
1. ASIP	*1620b*	*300 Mbps*
	1620b (WiMAX)	*100 Mbps*
	2304b (WiMAX)	*62 Mbps*

Low density parity check codes

FPGA based hardware architectures



the total delay path for updating the var nodes (R3) register values in case of 1 decoding iteration is

$T = u+v$ (clock cycles)

represents the number of 1 values within the H lines

the number of clock cycles necessary for $Sum2_j$ addition, respectively

$T = 10$ in case of WiMAX standard

WiMAX standard

$M = 576$ codeword length

$N_{iterations} = 10$ the number of iterations for the decoding process

$F_{clk} = 350\ MHz$ the frequency of the FPGA based decoder

Decoder throughput estimation

$$Throughput = \frac{M \cdot f_{clk}}{N_{iterations} \cdot T} \approx 2GHz$$

Conclusions

- Two applications were presented
  - Microarray image processing embedded system
  - LDPC decoder implementation
- FPGA Technology
  - Iterative algorithms
  - Increased data content
  - Real time system
  - Efficient implementations for high performance computing applications